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Penelope Test Plan - Revision v6.1 - 24 April 2008

This Document describes the methodology for testing the HPSDR Penelope Project Exciter board.

1 Test Fixture Description

There are two test fixtures, one for each of the two tests performed on the Penelope Board.

1.1 Test #1a Fixture Description

The JTAG test fixture consists of an empty Atlas Backplane (no loopback cable). Power is supplied to the board under test via the Atlas Backplane through an ATX connector by a PicoPSU-60-WI 60W. The PicoPSU is an ATX style power supply that receives its power from a nominal 12VDC source. The PicoPSU power supply can be purchased at http://www.mini-box.com/

A PC is used to run Altera Quartus II that uses a USB Blaster to load the FPGA in JTAG mode.

The on-board LEDs are used as pass/fail indicators for all tests.

1.2 Test #1b Fixture Description

The Loopback test fixture consists of an Atlas Backplane populated with a loopback cable. Power is supplied to the board under test via the Atlas Backplane through an ATX connector by a PicoPSU-60-WI 60W. The PicoPSU is an ATX style power supply that receives its power from a nominal 12VDC source. The PicoPSU power supply can be purchased at http://www.mini-box.com/

A PC is used to run Altera Quartus II that uses a USB Blaster to load the serial PROM in Active Serial mode.

The on-board LEDs are used as pass/fail indicators for all tests.

1.3 Test #2 Fixture Description

The RF/Codec test fixture consists of an Atlas Backplane populated with Ozy and Penelope boards. Power is supplied to the individual boards via the Atlas Backplane through an ATX connector by a PicoPSU-60-WI 60W. The PicoPSU is an ATX style power supply that receives its power from a nominal 12VDC source. The PicoPSU power supply can be purchased at http://www.mini-box.com/

A PC is used to run a Windows batch file (Initozy11a.bat) that loads initialization commands to the Ozy board. The same PC starts an instance of the Flex-Radio PowerSDR console that is has been modified for use with the Penelope board.

The PowerSDR console is required to command the Penelope board.

2 Test Fixture Hardware

2.1 Test Fixture 1a

Test fixture #1a uses the following additional hardware:

- An Altera USB Blaster to program the FPGA on the Penelope board.

2.2 Test Fixture 1b

Test fixture #1b uses the following additional hardware:

- An Altera USB Blaster to program the serial PROM on the Penelope board.

- An Atlas loopback cable. (This is the same cable that is used for Ozy testing.)
- A 10-pin ribbon loopback cable for P3 with pins 1 and 9 shorted.
- A DB25 loopback header for J6.

2.3 Test Fixture #2

Test fixture #2 uses the following additional hardware:

- A USB cable to connect the Ozy board to the PC running the PowerSDR console.
- A dummy load capable of continuously dissipating 1W of RF power.
- A microphone capable of driving the TLV320AIC23B codec on the Penelope board.
- A momentary PTT switch with the output wired to the ring of a 1/8" male stereo connector.
- An adapter cable to connect the microphone and PTT switch to the 1/8" stereo J4 connector on Penelope. The adapter cable has two 1/8" mono female connectors connected by a "Y" interface to one 1/8" stereo male connector.

3 Test Software

In order to perform testing it is necessary to download and install the following software.

3.1 USBIO or libusb-win32

The libusb-win32 driver set is preferred and is available from the www.sourceforge.net website. USBIO is available for download from www.flex-radio.com.

3.2 A Penelope enabled PowerSDR folder

PowerSDR is not automatically "installed" in Windows. Instead a folder with a Penelope enabled version of PowerSDR.exe and all other required files is copied into Windows. PowerSDR.exe is then run from that folder. A special version (1.10.4+ base SVN 2025) of PowerSDR is required for testing Penelope. This version of the PowerSDR file folder is available at www.hpsdr.org in the SVN repository.

After the software installation, create desktop shortcuts to the initozy11a.bat and PowerSDR.exe files and place them on the PC Desktop. Modify the PowerSDR shortcut by adding the expression:

"--ignore-pp-ppt"

after the "/$PATH$/PowerSDR.exe" in the properties pane of the shortcut. This statement will keep the absence of an Ozy to SDR-1000 parallel port connection from turning on the external PTT function.

3.3 PowerSDR Files

The PowerSDR files that are required to configure and run Ozy and Penelope are listed below:

ADODB.dll
CATStructs.xml
DttSP.dll
fftw_wisdom.exe
wisdom
HPSDR_USB_LIB_V1.1.dll
Initozy11a.bat*
Interop.ADOX.dll
JanusAudio.dll
msadox.dll
Ozy_Janus.rbf
ozyfw-sdr1k.hex
PA19.dll
PortTalk.dll
porttalk.sys
power.csv
PowerSDR.exe
PowerSDR.mdb

libfftw3f-3.dll
libusb0.dll
load_firmwareV1.1.exe
morsedef.txt
*The current version is Initozy11.bat
pthreadVC.dll
sleep.exe
upload_fpgaV1.1.exe
write_I2cV1.1.exe

4 Hardware Setup

4.1 Test Fixture #1a

Connect the USB Blaster to a USB port on the computer.

Connect an ATX power supply connector to the Atlas backplane.

4.2 Test Fixture #1b

Plug in the Atlas loopback cable to J1 (connector with few wires) and J3 (connector with many wires).

Connect the USB Blaster to a USB port on the computer.

Connect an ATX power supply connector to the Atlas backplane.

4.3 Test Fixture #2

Connect a USB cable from the PC to the USB connector on the Ozy board.

Attach the dummy load to the RF Connector on the Penelope board.

Connect an ATX power supply connector to the Atlas backplane.

5 Software Setup

5.1 libusb-win32 or USBIO Installation

Download and install libusb-win32 per its included readme file. If you have ever used the PowerSDR USB Adapter cable you may already have the required files installed on your PC.

5.2 Power SDR Initialization and Configuration

Double-Click on the PowerSDR Shortcut on the Desktop. The Startup Wizard will ask a number of questions. In response:

- Model: SDR-1000
- RFE Expansion Board: No
- External Clock Option: No
- USB to Parallel Adapter: No
- Sound Card: HPSDR Janus/Ozy (USB2)

Verify that the top panel of the PowerSDR console shows the message ***PP PTT disabled*** on it.

From the main drop down menu in PowerSDR open the HPSDR Setup Window (Setup ->General->HPSDR). In the “HPSDR Hardware Present” frame check the box Penelope. In the “10 MHz Clock Source” frame click the Penelope Radio Button. In the “122.8 MHz Clock Source” frame click the Penelope Radio Button. In the “Mic Source” frame click the Penelope Radio Button. Click on the Transmit tab at the top of the menu. In the Tune Frame set the Power level at 100. Close the menu by clicking the OK button.

Set the frequency of the PowerSDR console to 7.200 MHz. This is an arbitrary setting. Any frequency that allows full power transmit will work equally well. Set the Transmit Profile to Conventional. Increase the Microphone Gain to 16. Set the Display Mode to Scope. Shut down PowerSDR.

6 Penelope Testing

6.1 Penelope Test #1a and #1b Summary

1. Power LED (no test required)
2. LED 2 (122.88MHz Osc)
3. LED 3-7 (rotate when all tests pass)
4. U8 FPGA serial EPROM
    a. program through P2
    b. load FPGA using active serial mode
5. Load FPGA through JTAG header HDR2
6. Analog test: J6, U16 (DB25 loop-back)
7. PIO test: U18, U12-U14 (DB25 loop-back)
8. PIO Test: PTT out and PTT in
9. Atlas Bus interface
    a. A[2:22], A[24:25], A[27], A[29], A[31]
    b. C[2:22], C[24:25], C[27], C[29], C[31]

6.2 Penelope Test #2 Summary

1. LED 1 (Power)
2. LED 7 (FPGA Code Loaded)
3. U9 circuitry (VFWD Power Sensing)
4. LED's 2,3,4,5,6 (RF Power Sensing Circuit)
5. J4 (MIC Connector)
6. U6 (Power Amplifier)
7. U7 (DAC)
8. U10 (Codec)
9. JP2, JP3 and Internal Filter Assembly
10. FPGA PTT input
11. JP4 (PTT Selector)
12. JP5 (MIC Bias Selector)
13. JP6 (MIC AUD Selector)
14. U16 AIN5 (FWD Power Detect)
15. J5 (RF Out)

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6.3 Penelope Test Procedure #1a

1. Inspect PCB and serial number label
2. Install jumpers
    a. JP2 short pins 1-2 (right)
    b. JP3 short pins 1-2 (right)
    c. JP4 short pins 1-2 (top)
    d. JP5 short pins 2-3 (bottom)
    e. JP6 short pins 2-3 (bottom)
    f. JP7 short pins 1-2 (Last JTAG)
    g. JP8 (config B) short pins 1-2 (top)
    h. JP9 (config A) short pins 2-3 (bottom)
    i. JP10 short pins 1-2 (I2C Bypass)
    j. JP11 short pins 1-2 (I2C Bypass)
3. Plug Penelope into Atlas backplane in any slot
4. Plug byte blaster onto P3 and power up Atlas backplane
5. Load PennyTestImage.sof using JTAG and verify that LED2 flashes and LED3-7 stay on
6. Power down Atlas backplane
7. move jumper JP8 (config B) to short pins 2-3 (bottom)

6.4 Penelope Test Procedure #1b

1. Plug Penelope into Atlas backplane between loopback connectors
2. Plug loopback plug onto J6
3. Plug loopback cable onto P3
4. Plug byte blaster onto P2 and power up Atlas backplane
5. Load PennyTestImage.pof using AS and verify that LED2 flashes and LEDs 3-7 rotate
6. Load penelope.pof using AS and verify that LED1 and LED7 are lit
7. Power down Atlas backplane and remove loopbacks from P3 and J6

6.5 Penelope Test Procedure #2

1. Verify Jumpers:
    a. JP2 short pins 1-2 (right)
    b. JP3 short pins 1-2 (right)
    c. JP4 short pins 1-2 (top)
    d. JP5 short pins 2-3 (bottom)
    e. JP6 short pins 2-3 (bottom)
    f. JP7 short pins 1-2 (Last JTAG)
    g. JP8 (config B) short pins 2-3 (bottom)
    h. JP9 (config A) short pins 2-3 (bottom)

   i. JP10 short pins 1-2 (I2C Bypass)
   j. JP11 short pins 1-2 (I2C Bypass
2. Plug the Penelope board into the Atlas backplane
3. Connect the microphone and PTT adapter cable to J4.
4. Connect a dummy load to J5.
5. Power up the Atlas backplane
6. Verify LED's D1 and D7 on Penelope are lit
7. Double-click on the Initozy11a.bat shortcut on the PC desktop
8. Verify that on the Ozy board LED's D5-D8 and D12 are lit and that LED's D9 and D10 are flashing.
9. Start the PowerSDR Console.
10. Click the TUN button on the PowerSDR Console.
11. Verify that LED's D1-D5 and D7 on Penelope are lighted.
12. Click on the TUN button to turn it off.
13. Press the PTT Switch and speak into the microphone.
14. Verify that the display window on the PowerSDR console is showing a speech pattern.
15. Verify that LED's D1 and D7 are on steady and that D3-D7 are lighted in proportion to the amount of audio drive.
16. Power down Atlas backplane.

6.6 Package PCB for Shipment

Place the board in an antistatic bag and seal.